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OPENCORE NMR: Open-source core modules for implementing an integrated FPGA-based NMR spectrometer

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Abstract

A tool kit for implementing an integrated FPGA-based NMR spectrometer [K. Takeda, A highly integrated FPGA-based nuclear magnetic resonance spectrometer, Rev. Sci. Instrum. 78 (2007) 033103], referred to as the OPENCORE NMR spectrometer, is open to public. The system is composed of an FPGA chip and several peripheral boards for USB communication, direct-digital synthesis (DDS), RF transmission, signal acquisition, etc. Inside the FPGA chip have been implemented a number of digital modules including three pulse programmers, the digital part of DDS, a digital quadrature demodulator, dual digital low-pass filters, and a PC interface. These FPGA core modules are written in VHDL, and their source codes are available on our website. This work aims at providing sufficient information with which one can, given some facility in circuit board manufacturing, reproduce the OPENCORE NMR spectrometer presented here. Also, the users are encouraged to modify the design of spectrometer according to their own specific needs. A home-built NMR spectrometer can serve complementary roles to a sophisticated commercial spectrometer, should one comes across such new ideas that require heavy modification to hardware inside the spectrometer. This work can lower the barrier of building a hand-made NMR spectrometer in the laboratory, and promote novel and exciting NMR experiments.

Keywords: OPENCORE NMR; Spectrometer; Field-programmable gate-array (FPGA); Core modules

1. Introduction

Recently the author has developed a home-built NMR spectrometer with a design concept of fully exploiting an field-programmable gate-array (FPGA) [1]. An FPGA chip is a semiconductor device composed of a large number of programmable logic gates, in which a number of digital circuits, called as core modules, can be built by writing codes in one of hardware description languages such as VHDL and Verilog. FPGA development is attractive in the sense that (i) a core module is reusable once it has been developed, (ii) the individual core modules built inside an FPGA chip run in parallel, (iii) modules built inside an FPGA can be overwritten as many times as necessary, and (iv) a personal computer (PC) and a download cable suffice for FPGA development. In Ref. [1], an integrated FPGA-based NMR spectrometer has been presented, in which a single FPGA chip does all the digital jobs required for an NMR spectrometer, including a pulse programmer (PPG), a direct-digital synthesizer (DDS), a digital receiver composed of a digital quadrature demodulator and a digital low-pass filter, and PC interfaces for command/data transfer. This spectrometer has three rf channels, each of which is capable of modulating the amplitude, phase, and frequency of rf irradiation at up to 400 MHz.

This work describes the principle of operation of this integrated FPGA-based NMR spectrometer together with some experimental demonstrations, showing that the spectrometer presented here is of practical use for studying molecular structure and dynamics. This paper serves as a summary which helps the interested readers to understand the principle, and minute details such as the VHDL source codes, the precise circuit diagrams and board drawings of

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the peripheral devices, etc., are available on our web site [2]. By fully describing this open-source FPGA-based NMR spectrometer, which is referred to as the OPENCORE NMR spectrometer henceforth, this work encourages the potential users to not only utilize this spectrometer in their daily research activities, but also modify the system according to the users' own specific needs.

This work does not mean to compete against commercial NMR spectrometers, which are very carefully designed and well built. In fact, performance of the commercial spectrometers are so high that any modern standard NMR techniques can be implemented without difficulty. Note, however, that such standard techniques today were once innovative at the time of development, some of which had come along with heavy extension or modification to hardware. Since NMR is an exciting field of science in which remarkable progress has never declined since its birth decades ago, and is likely to continue, this work aims at stimulating future's pioneering works in the NMR community by lowering the barrier of building a modifiable home-built spectrometer [3–8], so that one can be prepared for putting exciting ideas which might happen at any time into practice.

The FPGA chip used in the current OPENCORE NMR spectrometer is EP2C70F672C8, which is one of "Cyclone II" device family by Altera [9]. Its 27 × 27 mm package has ~70 k logic elements, ~1 M RAM bits, 150 multipliers, 4 PLLs, and 622 I/O pins.

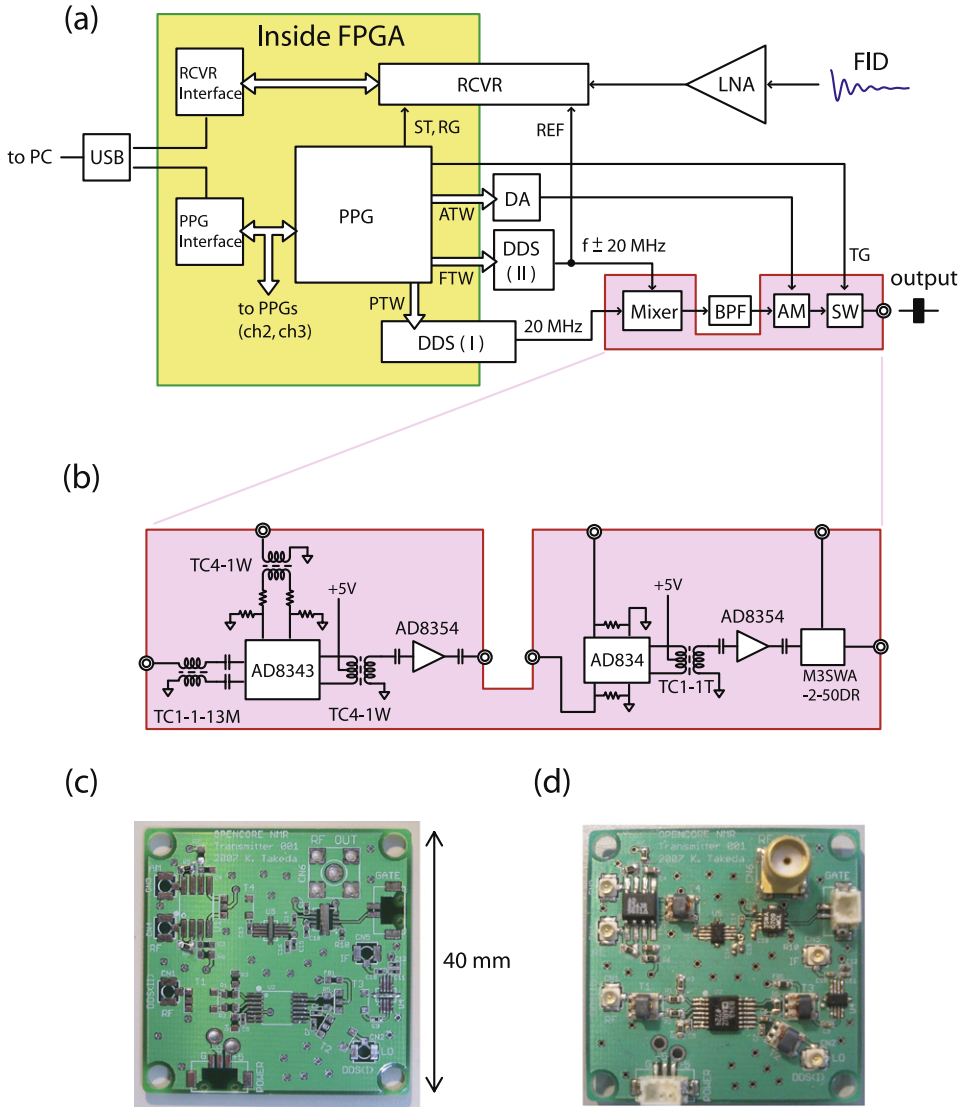

Fig. 1. (a) A block diagram for a receiver and one of three RF transmitter channels of the OPENCORE NMR spectrometer. The glossary is as follows: PPG, pulse programmer; DDS, direct digital synthesizer; AM, amplitude modulator; SW, switch; RCVR, receiver; FTW, frequency-tuning word; PTW, phase-tuning word; ATW, amplitude-tuning word; TG, transmitter gate; RG, receiver gate; ST, sampling trigger. Modules inside the area designated by a yellow rectangle are built inside a single FPGA chip. (b) A circuit diagram for each of the three rf transmitters corresponding to the red area of the block diagram in (a), which is implemented on a 40 × 40 mm circuit board shown in (c–d). The board was designed with a CAD soft and the components were hand-soldered.

2. Architecture of OPENCORE NMR

Fig. 1(a) describes a functional diagram of a transmitter for one of three rf channels and a receiver. In the present architecture of OPENCORE NMR, two rf sources, denoted by DDS(I) and DDS(II), are used for each rf channel. DDS(I) is phase-tunable and frequency-fixed at 20 MHz, while DDS(II) is frequency-tunable and phase-fixed. In order to generate a signal with an intended frequency f, the output frequency of DDS(II) is set to either $f + 20$ or $f - 20$ MHz. The signals from DDS(I) and DDS(II) are sent to a mixer (AD8343, Analog devices [10]), which generates the frequency f with an additional image frequency at $f \pm 40$ MHz together with several spurious signals. After eliminating the irrelevant frequencies by passing the signal through a home-built band-pass filter (a separate filter is necessary according to the frequency in interest), the signal is then amplitude-modulated with a multiplier (AD834, Analog devices [10]), and finally pulse-modulated with an rf switch (M3SWA-2-50DR, Mini-circuits [11]) to generate pulses. The phase, frequency, amplitude as well as the transmitter gate, power-amplifier unblanking, etc., are controlled by a pulse programmer (PPG) described in Section 3.

Although the block diagram in Fig. 1(a) itself describes a well known strategy for implementing an NMR spectrometer, the emphasis here is on clear distinction between the *digital* and *non-digital* operations. The digital jobs depicted inside the yellow area in Fig. 1(a) have been implemented inside the FPGA chip. In this figure, DDS(I) and RCVR cross over the FPGA boundary, meaning that they consist of both digital and analog circuitries.

The analog components of the transmitter designated by the red area in Fig. 1(a) are described in more detail in Fig. 1(b). As shown in Fig. 1(c)–(d), they are implemented on a 40×40 mm circuit board. The principle of signal acquisition in the receiver module denoted by RCVR in Fig. 1(a) will be described in Section 5.

In the current design of the OPENCORE NMR spectrometer, a Cyclone II (EP2C70F672C8) breadboard (ACM-201-70C8, HUMANDATA [12]) is used, which is shown in Fig. 2(a). This board has a size of 86×54 mm and is equipped with a 30 MHz crystal oscillator. Data transfer is possible through its 306 I/O ports on surface mount connectors (FX10, Hirose). The 30 MHz clock drives 2 PLLs inside the Cyclone II chip for generating clock signals at 20, 80, 100, and 160 MHz used both for the core modules built inside the FPGA chip and for the external AD/DA converters used in the RCVR, DDS (I), and amplitude-modulation modules. For stable high-speed data transfer between the FPGA chip and the peripheral AD/DA converters, it is desirable to put them as close to the FPGA chip as possible. Accordingly, the Cyclone II breadboard is docked with a 100×80 mm mother board on which 6 DA converters (3 for DDS(I), 3 for amplitude modulation for the three rf channels) and one AD converter for NMR-signal acquisition are implemented, as shown in Fig. 2(b). Also, the other modules are put around the FPGA mother board so as to minimize the cable length. For modification and tune-up purposes, most connectors are designed to be accessible from the top of the system, and circuit-board stacking was avoided. Such a design concept resulted in, after some trial and error, an overview of the OPENCORE NMR spectrometer as shown in Fig. 2(c).

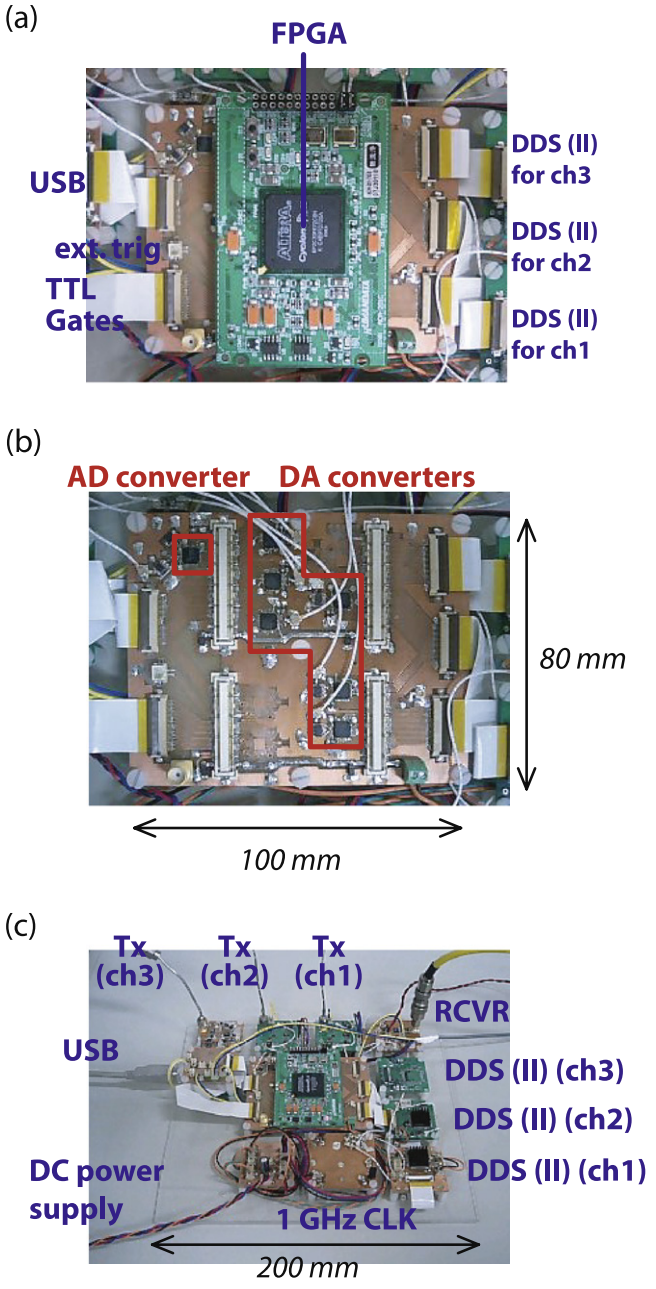

Fig. 2. (a) A Cyclone II FPGA breadboard (ACM-201, HUMANDATA inc.) docked with a mother-board shown in (b), on which an AD converter (AD9245BCPZ-80, Analog Devices) for RCVR, 6 DA converters (AD9740ACPZ, Analog Devices) for DDS (I) and amplitude modulation in each of the three rf channels, and 0.5 mm pitch FPC connectors for digital data transfer are mounted. (c) A snapshot of an OPENCORE NMR spectrometer.

3. Pulse programmer (PPG)

An NMR PPG is a device having a number of digital output ports used to control, e.g., rf amplitude, phase, frequency, transmitter gate, power-amplifier unblanking, receiver gate, sampling trigger, and so on [13–19]. In some cases, it is also required that the PPG can be triggered from an external device to operate in synchronous with, for instance, rotor signals. One or a set of the output ports is assigned to a peripheral device, which is to be controlled in accordance with the sequence programmed by the user. In OPENCORE NMR, three identical PPGs are employed

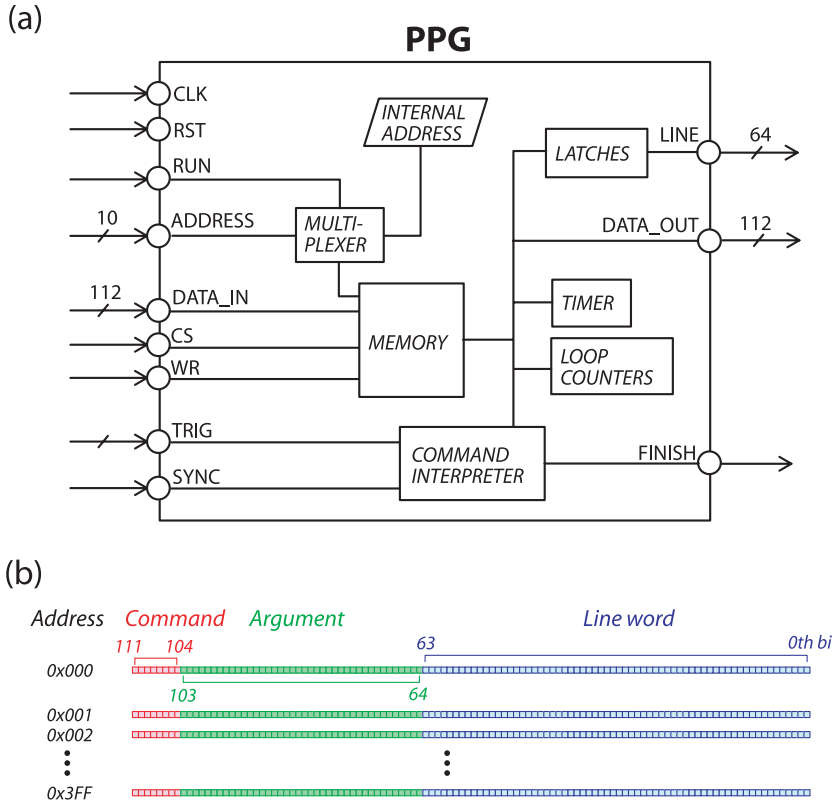

Fig. 3. (a) A schematic diagram for one of the three PPGs built inside the FPGA chip by writing hardware description codes in VHDL. (b) Memory structure of the PPG. Each address stores a set of 112 bits, which is divided into three parts: a command that the PPG obeys, an argument whose role depends on the command, and a line word specifying the logic level at each of the 64 output ports.

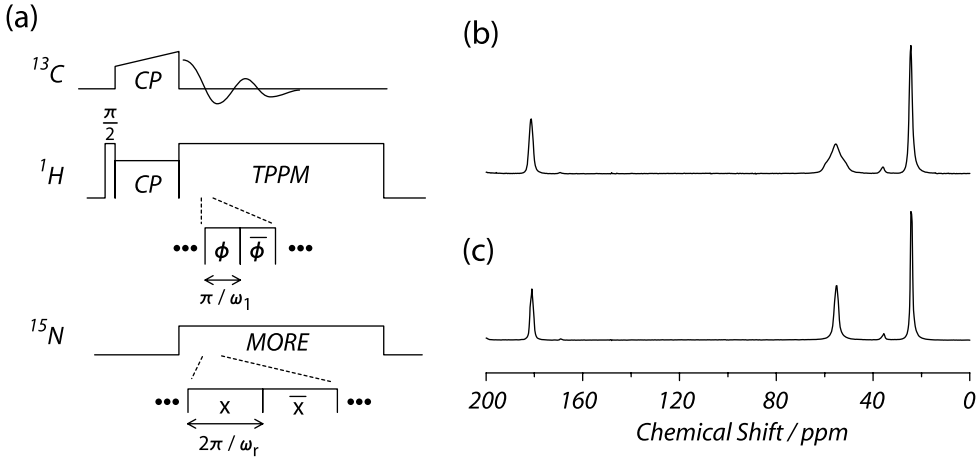

Fig. 4. (a) A pulse sequence of the MORE (MOdulatory REsonance) experiment [20] for heteronuclear dipolar recoupling between a pair of ^{13}C and ^{15}N spins under TPPM ^{1}H decoupling. (b) ^{13}C MAS spectrum obtained with the OPENCORE NMR spectrometer using the pulse sequence described in (a) in a polycrystalline sample of ^{13}C, ^{15}N-labeled l-alanine in a magnetic field of 7 T. The phase-modulation frequency of rf irradiation at the ^{15}N spin was adjusted to the sample spinning frequency $\omega_r/2\pi$ of 10940 Hz, and its amplitude was set to $\sim 2.3\omega_r/2\pi$ for attaining the maximum recoupling efficiency. During ^{13}C signal acquisition, TPPM decoupling was applied at the ^{1}H rf channel with $\phi = 10^\circ$ and $\omega_1/2\pi = 100$ kHz. All the three rf channels in the OPENCORE NMR spectrometer operated asynchronously during the signal acquisition. The signal was accumulated over 100 times. For comparison, a ^{13}C MAS spectrum without ^{15}N irradiation is shown in (c).

inside an FPGA chip for up to triple resonance experiments, each of which is assigned to control over the individual rf channel. Rather than a single PPG with many output bits, the three parallel PPGs have been chosen so as to take advantage of the concurrent property of FPGA, which enables asynchronous operation in a natural way.

3.1. Inside a PPG module

The design of the present PPG is based on a prototype developed by Prof. Takegoshi at Kyoto University (private communication). It operates at a clock frequency of 100 MHz and has a 40-bit timer counter and 64 line output ports. Thus, it can count with a time resolution of 10 ns up to 10 ns $\times 2^{40} > 10^4$ s. Also, one 40-bit loop counter and two 16-bit loop counters are incorporated. These loop counters can be nested so that an iteration of up to $2^{40} \times 2^{16} \times 2^{16} = 2^{72}$ times is possible.

As depicted in Fig. 3(a), the PPG module is equipped with a memory, which is accessible from an outside module via the ADDRESS, DATA_IN, CS (Chip Select), WR (WRite), and DATA_OUT ports. Two possible operation modes exist in the PPG: standby mode and run mode. The mode selection is indicated externally by setting the RUN port; when the RUN port is set to logic high (low), this module operates in the run (standby) mode.

In the standby mode, it is possible to modify the memory content by accessing the ports ADDRESS, DATA_IN, CS, and WR, so that the pulse program can be updated. Also, one can read the current memory content simply by specifying the ADDRESS bits, and checking the DATA_OUT port.

In the run mode, on the other hand, the internal address register becomes active, which means that one can neither specify an address nor update the memory content from the outside. Whenever the operation has been switched from the standby mode to the run mode by raising the RUN port, the internal address register is set to zero, at which the PPG module begins to operate by interpreting what is written in the current address of the memory.

In the current version of OPENCORE NMR, the PPG operates with a 100 MHz clock generated by a PLL module inside the Cyclone II FPGA device. To abort implementation, the RUN input port is to be restored to the low level. Under the run mode, the PPG checks the RUN input port every 10 ns, and when the low level is detected, terminates operation of the current pulse program immediately and deactivates all the output bits, irrespective of whether the pulse program has been finished or not.

3.2. Plural PPGs running in parallel: synchronous and asynchronous operations

The individual PPGs built inside the FPGA run in parallel. This concurrent property of the FPGA naturally meets the demand of an occasional situation where one or more rf channels are required to operate asynchronously. From the viewpoint of writing the separate binary pulse programming codes for the individual PPGs, there is nothing to do in particular for letting the PPGs operate asynchronously with respect to one another. However, in most part of typical NMR pulse sequences, the rf channels are to operate in a synchronous way. Moreover, the PPGs are sometimes required to re-synchronize after asynchronous operation. For this reason, the human-friendly pulse programming language mentioned below assumes synchronous operation by default, allowing optional asynchronous subroutines for occasional necessity. Also, the PPG is equipped with a re-synchronization mechanism.

As a demonstration of asynchronous operation, a MOdulatory REsonance (MORE) [20] ^{13}C–^{15}N dipolar recoupling experiment under magic-angle spinning (MAS) was carried out using the OPENCORE NMR spectrometer. In the MORE experiment described in Fig. 4, the ^{13}C signal was acquired under ^{1}H TPPM decoupling [21] and phase-modulated ^{15}N irradiation, where the frequency of phase modulation was adjusted to that of sample spinning. Since the pulse timings of the ^{1}H and the ^{15}N channels do not necessarily synchronize with each other, it is natural to let the PPGs of the individual channels operate asynchro-

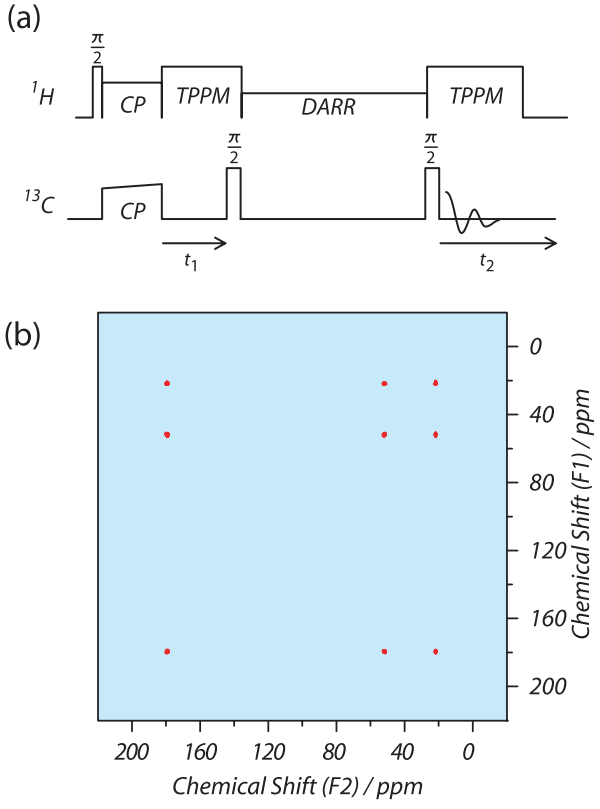

Fig. 5. (a) A pulse sequence for the 2D ^{13}C DARR exchange experiment. (b) A ^{13}C exchange 2D spectrum obtained using the OPENCORE NMR spectrometer with the pulse sequence in (a) in a polycrystalline sample of uniformly ^{13}C-labeled l-alanine in a magnetic field of 7 T. The mixing time was 20 ms, and the rotary-resonance recoupling was applied at the ^{1}H spins during the DARR period by irradiating rf with an intensity that coincides with the sample spinning frequency of 7 kHz.

nously. In this example, all the three rf channels were asynchronous during the acquisition period.

Fig. 5 demonstrates a ^{13}C DARR [22,23] experiment as another example of asynchronous operation with re-synchronization. After cross polarization, the ^{13}C magnetization freely evolves under ^{1}H TPPM decoupling, during which the ^{1}H and ^{13}C channels operate asynchronously. In this example, the two channels were commanded to re-synchronize after the t_1 period. After the DARR exchange period during which the PPGs of these two channels ran in synchronous with each other, the two rf channels went again in the asynchronous mode in order to implement the second TPPM decoupling during the detection t_2 period.

3.3. PPG-interface

The role of PPG-interface is to bridge between the PPGs and a computer console, and eventually, the user. For writing and readout purposes, the memory content at a given address carrying a command, an argument, and a line word is expressed by a hexadecimal number, and the corresponding character code is transferred between FPGA and PC. The PPG interface module receives character-based commands from PC, and if necessary, sends back character-based messages to PC. For character communication, a core module for EIA-232C (also often called as RS-232C) serial interface with a baud rate of 38400 bps was built inside the FPGA. Thus, data transfer between the pulse programmer and PC can be mediated either by an EIA-232C line driver chip or some EIA-232C emulators. In the OPENCORE NMR spectrometer, FT2232 (FTDI [24]) is used, which is a dual-channel USB line driver. One of its two channels is devoted for interfacing the pulse programmer in the 232 UART mode, while the other channel for FID data transfer using the 245 FIFO mode, which is faster than the 232 UART mode. Thus, both interfaces for pulse programming and for data acquisition are done through a single USB cable by using this dual line driver. The FT2232 communication board developed in this work and its layout are shown in Fig. 6(a) and (b).

The reason for choosing the EIA-232C communication protocol, which may seem to be rather obsolete nowadays, is because of its simplicity, availability, and thereby applicability to various purposes. Although the speed of data transfer in the 232 UART mode is relatively slower as compared to other modern interfaces, speed is not so critical in the process of sending pulse programs when the PPG is in the standby mode. Instead, in order for the present PPG to be applicable as a general-purpose pulse programmer with-

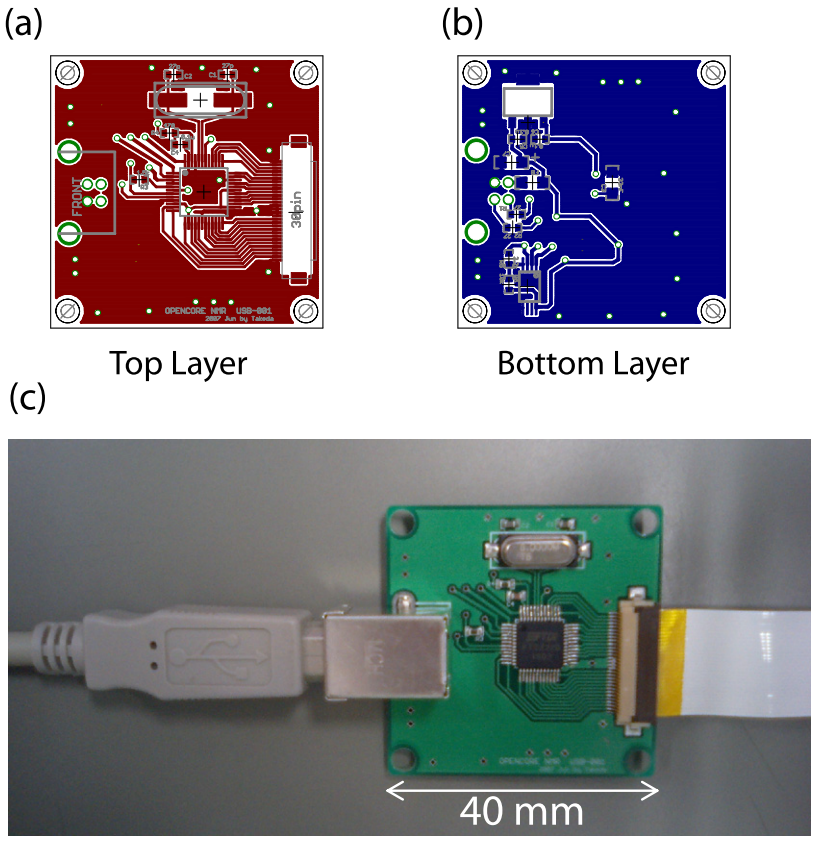

Fig. 6. The USB modules for data transfer between PC and the OPENCORE NMR spectrometer. On a 40 × 40 mm double-layered board shown in (a) and (b) implemented a FT2232 (FTDI) chip for dual-channel data transfer through a single cable. One channel is devoted for sending pulse-programming codes in the 232 UART mode, the other for transferring NMR signals in the 245 FIFO mode, (c) is a snapshot of the USB module.

out restriction to NMR, priority has been given to simplicity and availability.

3.4. Human-friendly pulse programming

From practical point of view, it would be rather tedious and time consuming to write a list of hexadecimal codes that the PPG obeys. Moreover, it would be quite hard to detect mistakes. Obviously, the natural and efficient procedure of pulse programming is to write a pulse program in a human-friendly language and let a computer program interpret it and generate a list of the corresponding hexadecimal codes. In this work, the pulse programming language developed by Takegoshi has been extended, and a class library has been developed that translates the human-friendly pulse program into the hexadecimal codes. The library provides a fail-proof environment, which automatically detects a number of possible artificial mistakes including syntax errors, out-of-range errors, and unclosed loops. The grammer of the human-friendly pulse programming is described on the web site together with various example codes such as one-pulse, CP, TPPM decoupling, and FSLG experiments [2].

4. Direct digital synthesizer (DDS)

4.1. DDS(I)

DDS is a means for generating signal waves by utilizing digital signal processing. The digital part of the phase-tunable and frequency-fixed DDS, denoted here as DDS(I), was built inside FPGA as a core module, while the non-digital parts, i.e., DA conversion and filtering, were employed outside the FPGA. For this reason DDS(I) crosses the boundary of the FPGA in the functional diagram in Figs. 1 and 7(a). On the other hand, the entire part of DDS(II) to be described in Section 4.2, has exceptionally been implemented outside the FPGA using a DDS-dedicated LSI in the current version of OPENCORE NMR, because the speed requirements were not met. The output level of a DA converter is updated in synchronous with a master clock. As a consequence of discrete change in the output voltage at clock rising edges, the output of a DDS circuitry contains signal components with the image frequencies in addition to the fundamental one. Usually, the output signal is passed through a filter to select one of either fundamental or image frequencies.

In the OPENCORE NMR spectrometer, DDS(I) operates at a clock frequency of 160 MHz, and generates a signal with a fixed frequency at 20 MHz. Fig. 7(b) shows a circuit diagram of the non-digital part of DDS(I). For the DA converter used was AD9740 (Analog Devices [10]), which has 10 bit resolution with the maximum update rate of 210 MHz. Its differential output is converted to a single-ended signal with an rf transformer (TC1-1T+, Mini-Circuits [11]). Fig. 7(c) shows the output signal from the transformer monitored on a digital oscilloscope. By passing the signal through a low-pass filter, the irrelevant frequency components can be eliminated, as demonstrated in Fig. 7(d).

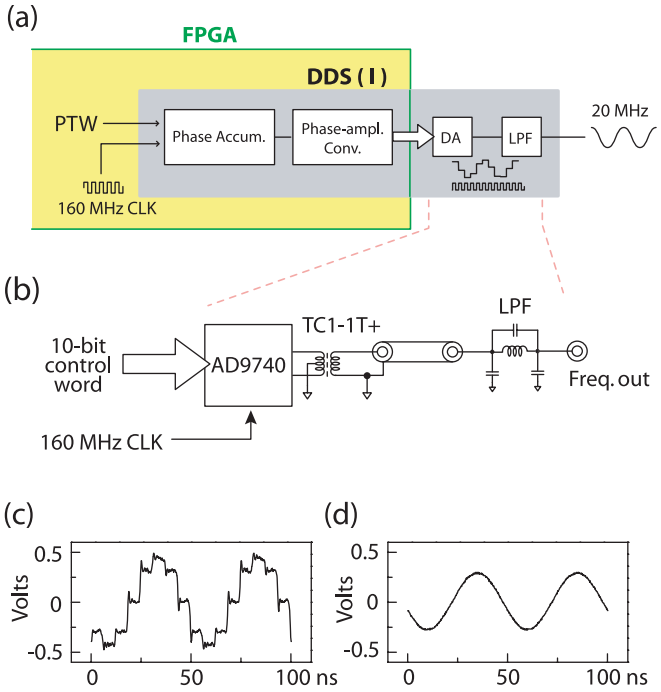

Fig. 7. (a) A block diagram of DDS(I) (frequency-fixed and phase-tunable DDS) in more detail than that shown in Fig. 1. (b) A circuit diagram for the non-digital part of DDS(I) built outside the FPGA. (c) Output of the DA converter monitored on a digital oscilloscope. The signal at 20 MHz is generated by the DDS circuitries inside the FPGA with a 160 MHz master clock. The unnecessary image frequencies can be eliminated by passing the signal through a low-pass filter, as demonstrated in (d).

By setting a 10-bit phase word, the phase of the signal from DDS(I) can be manipulated with respect to the output signal as it would be had the phase not been shifted. The 10-bit phase word (from 0x000 to 0x3FF in hexadecimal expression) determines the amount of phase shift within a range from 0 to 2π with a resolution of $2\pi/2^{10} \sim 0.0061$ rad $\sim 0.35°$. In order to sustain phase consistency between the transmitter and the receiver, the DDS(I) core module shares the master clock signal with

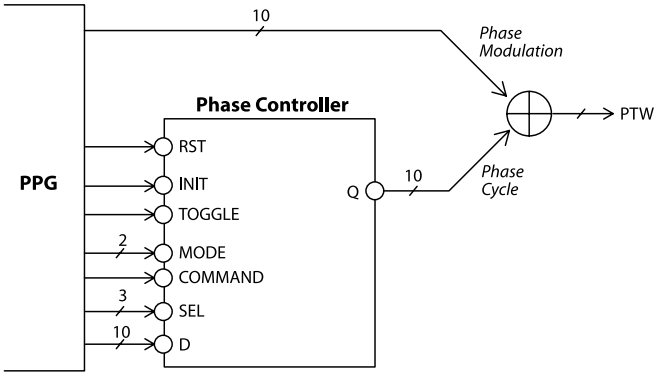

Fig. 8. A strategy for phase modulation and phase cycling.

the core module of the digital quadrature demodulator described in Section 5.1.

The actions of phase manipulation in NMR experiments are divided into two categories, i.e., phase modulation and phase cycling. The former is straightforward, which is used to specify a phase value at a certain timing. In phase cycling, a list of phase values is assigned at one or more specific timings during a sequence, and the individual phase value is taken every scans by rotation. In order to realize phase manipulation in both of these respects, phase controllers have been built for the individual rf channels. Since the phase controller uses only digital processing, it was built inside the FPGA as a core module. As schematically described in Fig. 8, the 10-bit phase tuning word (PTW) that is sent to the DDS(I) module is generated by adding two 10-bit phase words, one being the control word for phase modulation, the other representing an element of a phase cycle list. Although a carry occurs when the sum exceeds $2^{10}-1$, a carry holder is not necessary with the present design, where the periodic property is exploited by corresponding the full scale of the phase word with the 2π phase shift. Owing to this very design, discarding the carry bit is just equivalent to taking a modulo 2π, which makes no difference.

Seven phase cycles are available for each rf channel, and the individual cycle can store up to 32 phase values with 10-bit resolution. The 3-bit logic-vector word (1–7) at the SEL input port depicted in Fig. 8 specifies one of the seven phase cycles to be selected. Zero at the SEL input port deactivates the module. The phase cycle module consists of array of memories, and is controlled by the PPG module.

4.2. Frequency-tunable DDS (DDS(II))

For the phase-fixed and frequency-tunable DDS designated as DDS(II) in this work, a DDS-dedicated LSI, AD9858 (Analog Devices [10]) was employed, which operates at a clock frequency of 1 GHz. In principle, the maximum output frequency is limited by the Nyquist value given by half the clock frequency, while the realistic maximum frequency is ~ 0.4 times the clock frequency, i.e., $\sim 0.4 \times 1$ GHz ~ 400 MHz. Fig. 9 shows a circuit diagram, a board layout, and a photograph of DDS(II).

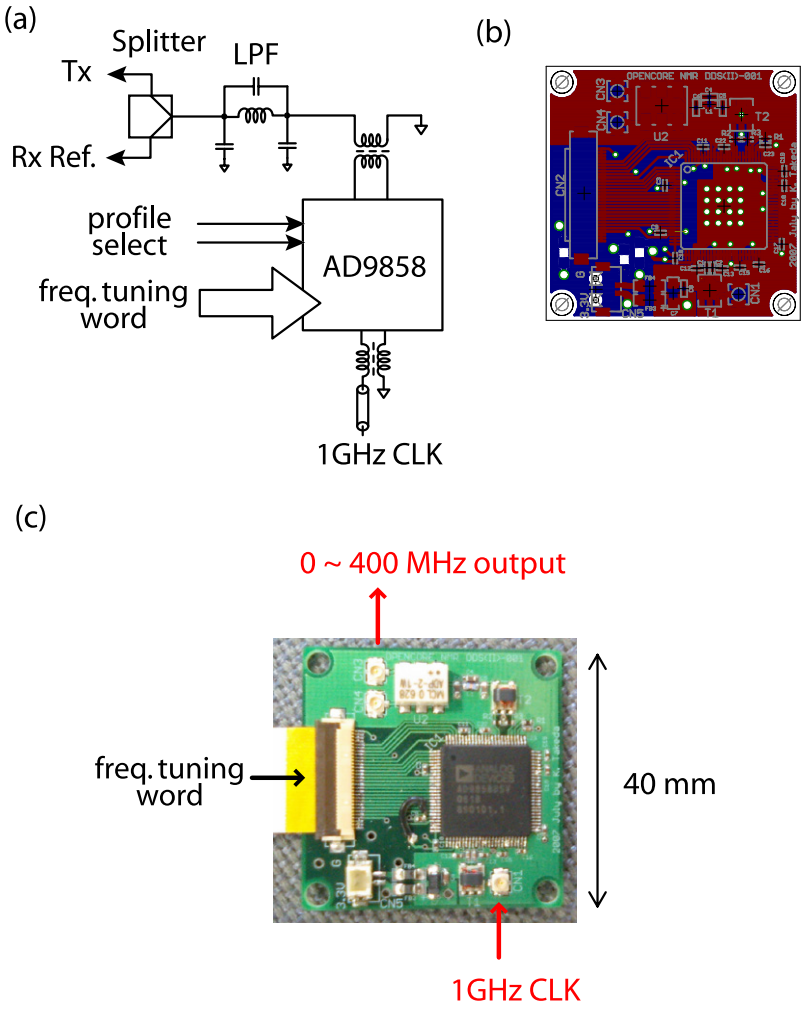

Fig. 9. (a) A circuit diagram, (b) a board design, and (c) a snapshot of DDS(II) (phase-fixed and frequency tunable DDS).

In AD9858, the output frequency is set by a 32-bit frequency-tuning word, determining the frequency resolution to be 1 GHz/$2^{32} \sim 0.23$ Hz.

Interestingly, AD9858 can hold four output frequencies, out of which one frequency is selected with a two-bit profile-select word (see Fig. 9). This feature enables a rapid frequency switching from one value to another by registering the frequencies to be used in advance of running a pulse sequence, and is thus suitable particularly for, e.g., FSLG experiments, which requires abrupt frequency jumps between two values together with phase inversion. On the other hand, for experiments requiring more than four frequencies, the frequency can be set by the 32-bit frequency-tuning word in the course of the sequence. Both of these two options for frequency modulation can be performed in the OPENCORE NMR spectrometer with appropriate pulse programming. As examples of frequency modulation by means of these two options, an FSLG-CRAMPS [25,26] experiment and NICP [27] and SADIS CP [28] experiments are demonstrated in Figs. 10 and 11, respectively.

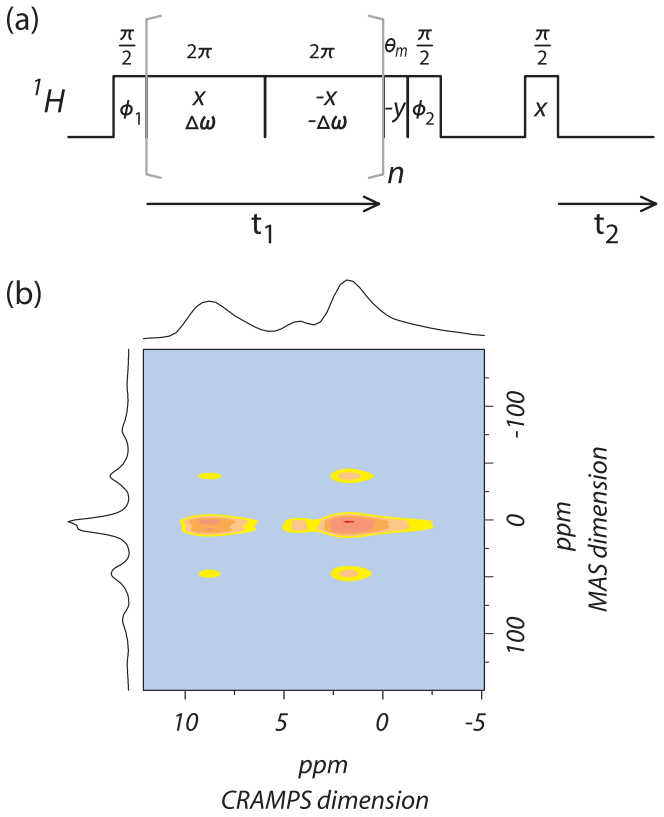

Fig. 10. (a) A pulse sequence for ^{1}H FSLG-CRAMPS. During t_1, the irradiation frequency is hopped between the two values together with phase inversion so that the antiparallel effective fields make the magic angle with respect to the static field. The phase ϕ_1 and acquisition phase were cycled as $(x, -x)$ and $(x, -x)$. For hypercomplex data acquisition during t_1, separate measurements are performed with $\phi_2 = (x, y)$. (b) A ^{1}H FSLG-CRAMPS spectrum obtained using the OPENCORE NMR spectrometer in a polycrystalline sample of l-alanine in a magnetic field of 7 T and at a spinning frequency of 11 kHz.

5. Signal acquisition

Inside the area designated by the gray rectangle in Fig. 12(a) described is the block diagram of the signal acquisition circuitry in more detail than that described in Fig. 1. The NMR signal (FID) is, after passed through a low-noise preamplifier, sent to the RCVR board shown in Fig. 12(b). On the RCVR board, the signal is demodulated by a mixer (AD8343, Analog Devices [10]) with the reference frequency of the DDS(II) module of the observation channel into the intermediate frequency (IF) at 20 MHz $- \Delta$, where Δ is the resonance-offset frequency of the NMR signal. The IF signal is then fed to an AD converter (AD9245BCPZ-80, Analog devices [10]), which digitizes the analog input signal at a sampling rate of 80 MHz with a dynamic range of 14 bits. As mentioned above in Section 2 and as shown in Fig. 2, the AD converter is mounted on the mother-board so as to minimize the physical length of the high-speed data-transfer line.

According to the design concept of the OPENCORE NMR spectrometer that digital jobs are left to FPGA, the digitized IF NMR signal is processed inside the FPGA chip until the signal is passed through the USB module toward PC, as schematically described in Fig. 12(a). The tasks to be processed inside the FPGA include digital quadrature demodulation, digital low-pass filtration, and signal accumulation and storage. That is, the IF signal at 20 MHz $- \Delta$ is digitally demodulated into in-phase and quadrature components having a frequency $(-\Delta + 20\ \text{MHz}) - 20\ \text{MHz} = -\Delta$. Then, each of the in-phase and the quadrature components of the signal is passed through a digital low-pass filter, and the processed data is stored with a specified acquisition phase, accumulated, and finally sent to a PC through the USB module described in Section 3.3.

5.1. Digital quadrature demodulator

As discussed in Ref. [1], the process of digital quadrature demodulation becomes quite simple when the AD sampling rate is exactly four times the demodulation reference frequency, as is the case for the OPENCORE NMR spectrometer, where the former and the latter are 80 and 20 MHz, respectively. This condition ensures that the multiplication factors $\sin(2\pi t \cdot 20\ \text{MHz})$ and $\cos(2\pi t \cdot 20\ \text{MHz})$ used in the demodulation process take only 0, 1, and -1 at the 80 MHz clock edge, greatly simplifying the arithmetic operations. Consequently, FPGA programming for building the digital quadrature demodulator of the functional diagram in Fig. 13(a) required only a multiplexer that passes the input data to the in-phase and quadrature outputs one after another with sign-inversion, as described in the diagram of Fig. 13(b).

5.2. Digital filter

The digital quadrature demodulator receives the digitized data points 80 M times a second and outputs the in-phase

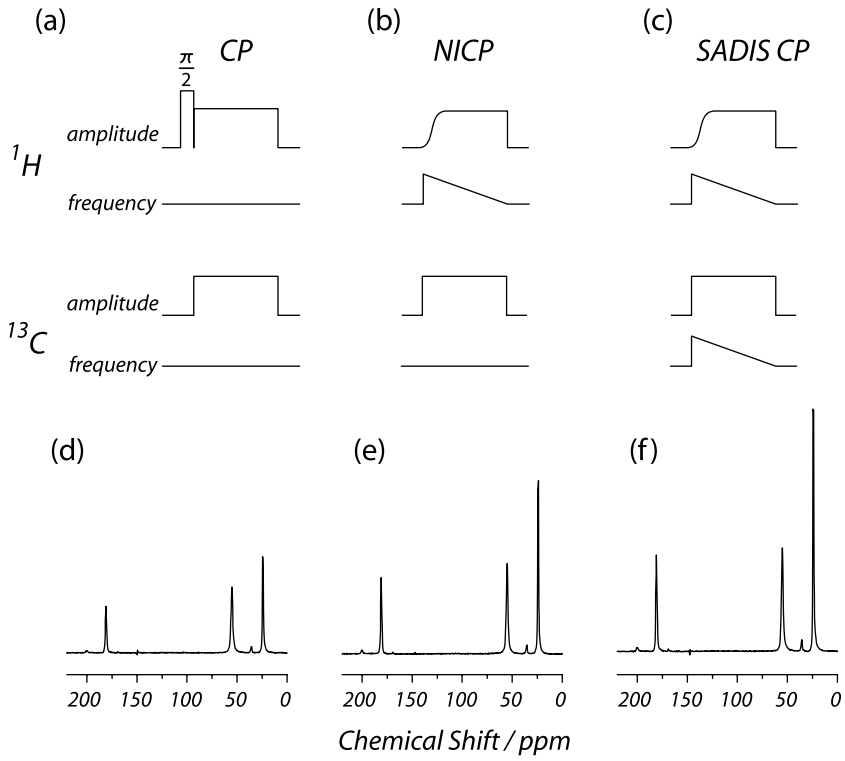

Fig. 11. (a–c) Pulse sequences for (a) the conventional Hartmann-Hahn CP, (b) NICP, and (c) SADIS CP experiments. In NICP, the initial $\pi/2$ pulse is removed and adiabatic frequency sweep is applied from far-off resonance toward on-resonance at the polarization-source (^{1}H) spin. In SADIS CP, the frequency sweeps are simultaneously applied at both the source and target (^{13}C) spins from far-off resonance toward on-resonance. (d–f): ^{13}C MAS spectra in a polycrystalline sample of ^{13}C labeled L-alanine in a magnetic field of 7 T enhanced by (d) the conventional Hartmann-Hahn CP with a contact time of 1.2 ms, (e) NICP with a frequency-sweep time of 1.2 ms and a frequency-sweep width of 100 kHz, and (f) SADIS CP with a frequency-sweep time of 1.2 ms and a frequency-sweep width of 100 and 120 kHz for the ^{1}H and ^{13}C channels, respectively. The individual spectra were obtained with their respective optimized experimental parameters. In NICP and SADIS CP, the frequencies were swept in 22 steps during polarization transfer.

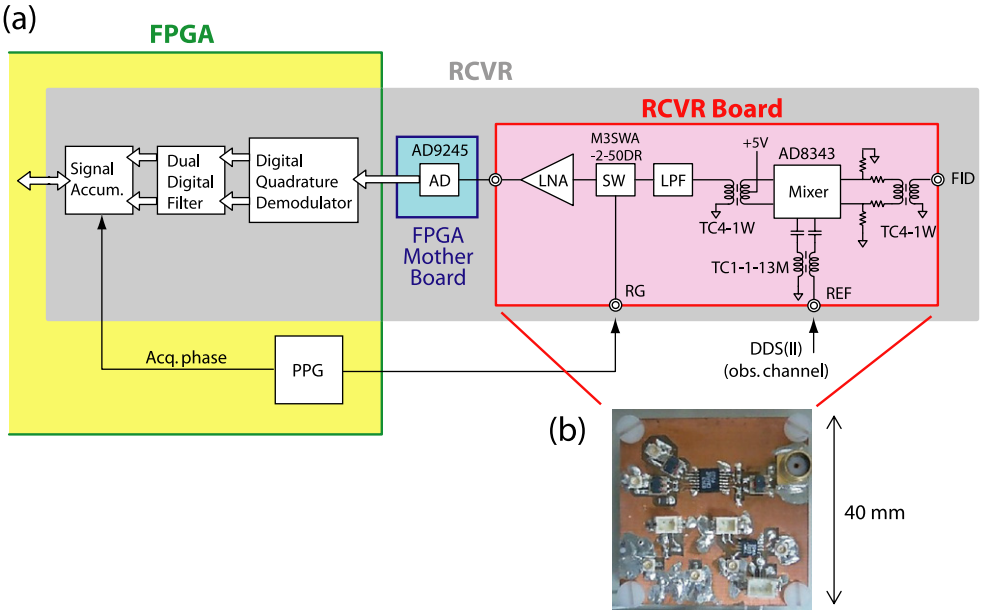

Fig. 12. (a) A block diagram of the signal acquisition circuitry (see Fig. 1(a)) described in detail. (b) A snapshot of the 40 × 40 mm RCVR board.

and quadrature components separately, each of which is refreshed at half the AD sampling rate. In most NMR experiments, on the other hand, the rate of data storage determined by inverse the spectral width is, at most, a few MHz. The oversampled data points can be used for digital filtering to get rid of frequency components lying outside

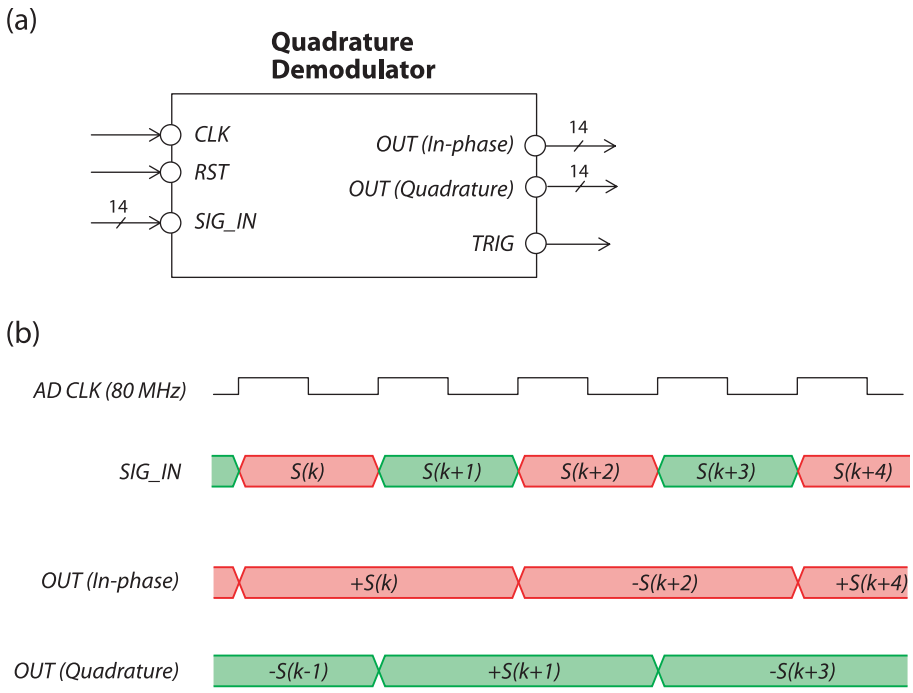

Fig. 13. (a) A functional diagram and (b) a timing chart of the digital quadrature demodulator of the OPENCORE NMR spectrometer.

the spectral width. For digital low-pass filtration of the in-phase and quadrature signals, a dual finite impulse response (FIR) filter is implemented inside the FPGA chip [1].

5.3. Signal accumulator

A memory module for storing the NMR signal is also prepared inside the FPGA. In the current OPENCORE NMR spectrometer, up to 8192 data points can be stored for each of the in-phase (real) and quadrature (imaginary) signals with one of four possible acquisition phases of x, y, $-x$, $-y$ (or equivalently, 0, 1, 2, 3) specified by the PPG.

The stored data can either be transferred to PC every scan or accumulated n times ($n < 64$) before data transfer. The latter option is particularly useful for experiments requiring a large number of signal accumulations with a very short repetition time less than 100 ms, because time interval required for data transfer would limit the repetition rate of the pulse sequence.

As an example shown in Fig. 14 is a ^{195}Pt NMR experiment in a platinum powder sample [29–31]. In this sample, the T_1 value of the ^{195}Pt spin was found to be less than 1 ms, and sensitivity is quite low because its spectral width as large as several MHz due to Knight shift distribution only allows partial excitation of the spin packets at a time, necessitating rapid signal accumulations over many times. In this example, the OPENCORE NMR spectrometer was used to implement a pulse sequence depicted in Fig. 14 (a) at a fixed frequency of 58.06 MHz for various external static fields. In order to cancel out the coherent transient noise from the refocusing π pulses, the phase of the first pulse and the

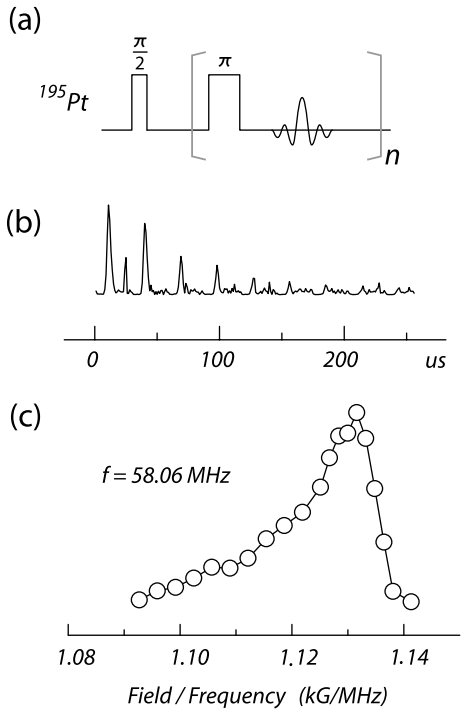

Fig. 14. (a) A pulse sequence for the CPMG spin-echo train experiment. (b) A ^{195}Pt spin–echo train obtained in a 100 mg platinum powder sample (Aldrich) at 77 K. The carrier frequency was 58.06 MHz, and the magnetic field was set to 6.56 T, corresponding to the resonance condition (field/frequency) of 1.13 kG/MHz. The signal was accumulated over 20,000 times with a repetition interval of 2 ms. The phase of the first pulse and the acquisition phase was cycled as (x, $-x$) while that of the second π pulse was fixed to y. The signals were accumulated inside the FPGA and transferred to PC every 63 scans. (c) The ^{195}Pt echo intensities plotted as a function of the external field.

acquisition phase was cycled as $(x, -x)$ and $(x, -x)$ while those of the π pulses were fixed to y [29], and the signals were accumulated over 63 times inside the FPGA before transferred to the PC through the USB module.

6. Summary

In this work has been described the principle of operation of the integrated FPGA-based NMR spectrometer, referred to as the OPENCORE NMR spectrometer, for the purpose of offering the NMR community to share one possible design of an operational home-built NMR spectrometer which can perform up to triple resonance experiments with the amplitude-, phase-, and frequency-modulation capability at up to 400 MHz. Since most digital parts have been implemented inside a single FPGA chip, the size of the system has become quite small, and the effort of reproducing the spectrometer has been considerably reduced as compared to the other designs.

Also, some demonstrations of the modern solid-state NMR techniques using the OPENCORE NMR spectrometer have been presented. On the other hand, for application to liquid samples where resonance-line widths can be less than a few Hz, care should be taken to use quite a stable clock source, because the apparent resonance line can be broadened due to clock-jitter. In order to deal with such a case, an optional SMA connector is equipped on the mother board, so that another stable clock signal can be fed to drive the PLL in the FPGA chip (modification to the FPGA programming is necessary accordingly). Nevertheless, when the resonance-line width is more than several Hz, as is the case for most solid-state NMR experiments, it was found that clock performance does not cause discernible disturbance in the spectra.

The author would like to be honest to claim that the OPENCORE NMR spectrometer presented here is not a perfect machine. As is the case for most open-source freewares, the design of the system will continue to be subject to change for better performance. Information as to the forthcoming upgrades will be announced on the website [2].

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