A radio-frequency source using direct digital synthesis and field programmable gate array for nuclear magnetic resonance

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A radio-frequency (rf) source for nuclear magnetic resonance (NMR) is described. With the application of direct digital synthesis (DDS), the rf source has the ability to yield rf pulses with short switching time and high resolution in frequency and phase. To facilitate the generation of a soft pulse, a field programmable gate array (FPGA) cooperating with a pulse programmer is used as the auxiliary controller of the DDS chip. Triggered by the pulse programmer, the FPGA automatically controls the DDS to generate soft pulse according to predefined parameters, and the operation mode of the pulse programmer is optimized. The rf source is suitable for being used as transmitter in low-field (<1 T) NMR applications, for example, magnetic resonance imaging and relaxation measurement. As a compact and low-cost module, the rf source is of general use for constructing low-field NMR spectrometer. © *2009 American Institute of Physics.* [doi:10.1063/1.3271379]

I. INTRODUCTION

The design of a radio-frequency (rf) source is critical to the development of a nuclear magnetic resonance (NMR) spectrometer. In addition to the frequency range and spectral purity, it is generally desired that the rf source has the ability to yield rf pulses with short switching time and high resolution in frequency and phase. The cost and complexity of a rf source are also considerable factors of the design.

In principle, frequency synthesis is achieved through three methods: analog mixing, phase locked loop, and direct digital synthesis (DDS).[1] With the development of modern electronic technologies, the DDS technique is becoming the most common choice for constructing rf source for an NMR spectrometer because it has the advantage of being able to control the frequency and phase of a rf signal digitally, rapidly, and precisely. For example, well-known frequency synthesizers, such as the Programmed Test Sources (PTS), Inc. (Littleton, Massachusetts) series devices, which incorporate the DDS technique, have been often utilized as rf source in several NMR spectrometers.[2–5] In recent years, DDS chips with high integration, i.e., complete-DDS, are used more often in NMR spectrometer design[6–8] for their low-cost and compactness.

Generating soft pulse for selective excitation is a fundamental function in NMR,[9] particularly in magnetic resonance imaging (MRI). There are several schemes adopted for soft pulse generation; for example, pulse programmer controls DDS directly,[6,10] or the output of DDS is modulated by the amplitude set by pulse programmer using an analog multiplier.[7]

For constructing low-field NMR spectrometer, some rf sources mentioned above seem complex (rf source and pulse programmer are integrated on a single chip);[7,10] as a result, these designs are hard to be utilized, and the cost is relatively high. Herein, a rf source suitable for soft pulse generation is described. The design has two key features: (1) a DDS chip is used to yield rf pulses and (2) a field programmable gate array (FPGA) under the control of pulse programmer (through its asynchronous bus) is used as the auxiliary controller. There are two operating modes: when a hard pulse is required, the pulse programmer controls the DDS directly, bypassing the FPGA; when a soft pulse is required, the pulse programmer first sets the relative parameters (rf frequency, update period, etc.) and modulation waveform, and then FPGA takes over the control and automatically manipulates the DDS to output soft pulse according to the configuration.

The DDS we employed is AD9852 (Analog Device, Inc., Norwood, Massachusetts) in which the highest system clock is 300 MHz; therefore, the frequency range of the output signal is from dc to approximately 135 MHz (0.45×300 MHz). Considering the spectral purity and amplitude of the output of AD9852, the application of rf source is focusing on low-field (<1 T) NMR, including MRI and relaxation measurement.

The presented design achieves short switching time and high resolution in frequency and phase of the rf pulse. Moreover, the design optimizes the operation mode of the pulse programmer by releasing it from frequently updating the registers of the DDS when generating soft pulse. Furthermore, the rf source is fit for many kinds of pulse programmers, for example, digital signal processor (DSP), FPGA, and personal computer. With the advantages of compactness and low-cost (the total price of chips is less than $120), the rf source is a good choice for the transmitter of low-field NMR spectrometer.

II. HARDWARE ARCHITECTURE

A block diagram of the rf source is shown in Fig. 1. A 32-bit floating-point DSP, TMS320VC33 (Texas Instruments, Inc., Dallas, Texas), works as the pulse programmer

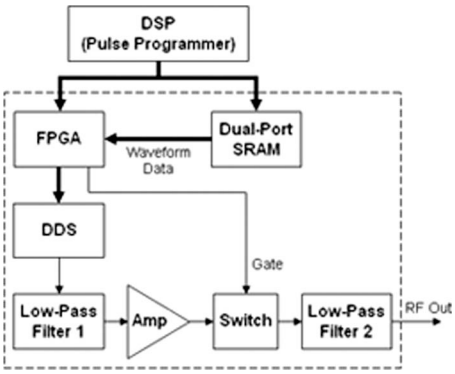

FIG. 1. Block diagram of the rf source.

of the NMR spectrometer. The DSP achieves a peak performance of 75×10^6 instructions/s and communicates with a personal computer through the development tool, XDS560, or other interface cards.

Before running the sequence, the DSP stores the phase and amplitude of the modulation waveforms of soft pulses into the dual-port static random access memory (SRAM). The chip employed here is CY7C026 (Cypress, Inc., San Jose, California) with a storage capacity of 16 $K\times16$ bit.

FPGA is composed of plentiful programmable logic gates and has the features of reconfigurable and concurrent. In the present design, the FPGA EP2C20F484 (Altera, Inc., San Jose, California), composed of 18752 logic elements and other hardware sources (Ref. 11) is utilized as the auxiliary controller of the DDS, in other words, the bridge between the DSP and DDS.

A block diagram of the FPGA is shown in Fig. 2. There are two key modules inside the FPGA: one is the control word, and the other is the operation core. Set by the DSP, the control word is used to produce the select signal for the multiplexer to decide the control of the DDS and the trigger signal of the operation core to generate soft pulse. The operation core—consisting of flip-flops, counters, and comparators—produces the address and control signals for the dual-port SRAM and DDS needed for soft pulse generation. The timing of the operation core depends on the reference clock and waveform parameters predefined by the DSP. Herein, the waveform parameters are parameters of the modulation waveform, including the update period of phase

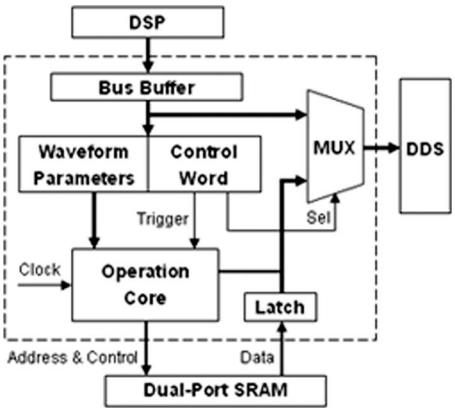

FIG. 2. Block diagram of the FPGA.

and amplitude of the DDS, storage location of the waveform in dual-port SRAM, and waveform length. After receiving the trigger signal, the FPGA periodically reads the modulation waveform from dual-port SRAM and then updates the registers of phase and amplitude of the DDS according to predefined parameters, thereby generating a soft pulse using the DDS.

The update period of phase and amplitude of DDS is programmable, ranging from 0.5 μs [the shortest period declared before is 1 μs (Ref. 12)] to approximately 80 μs in multiples of 20 ns. In the application of MRI, the shorter update period of DDS, the smaller spectrum distortion of the output soft pulse.

AD9852 (Ref. 13) is a complete-DDS chip that consists of a DDS core, digital multiplier (for amplitude modulation), digital-to-analog converter (DAC), clock circuit, resister file, and control interface. The highest system clock of AD9852 is 300 MHz; therefore, the frequency range of the output signal is from dc to approximately 135 MHz (0.45×300 MHz). AD9852 has registers of 48-bit frequency tuning word (FTW) and 14-bit phase offset word (POW), providing 1×10^{-6} Hz frequency resolution with 300 MHz system clock and 0.02° phase resolution; in addition, the amplitude modulation word (AMW) is 12 bit. When generating a single-tone signal, the total pipeline delay of the chip is less than 50 system clocks, allowing a short updating time of waveform parameters if the system clock is 300 MHz. The integrated 12-bit DAC has excellent dynamic range; for example, the narrowband spurious-free dynamic range of the output signal is about 82 dBc at 41 MHz (±1 MHz). Due to the characteristics of AD9852, i.e., high integration, ease-of-control and low price (less than $16), the rf source is rather compact and low-cost. However, the highest frequency (135 MHz) of the output signal will limit the application of AD9852.

Passing through low-pass filter 1, the output of AD9852 is amplified by an operational amplifier, herein OPA843 (Texas Instruments, Inc.) is employed, which has the characteristics of 800 MHz gain-bandwidth product, low input noise and harmonic distortion. The amplitude of the output signal of the rf source is 1 Vpp at 50 Ω impendence. To keep the amplitude stable, the closed-loop gain of the operational amplifier circuit has to vary with frequency because the baseband energy of the output of AD9852 decreases as frequency increases. The rf switch, SW-239 (Macom, Inc., Lowell, Massachusetts), with a 4 ns switching time and 56 dB isolation, is utilized to turn on and off the output signal under the control of DSP.

The rf source and the DSP have been implemented on a printed circuit board. Figure 3 shows the photo.

III. CONTROL PROGRAM

One program, written in TMS320C3X assembly language, is executed by the DSP to generate rf pulse. Subroutines for generating hard pulse and soft pulse are described below.

When a hard pulse is needed, the DSP first sets the control word of the FPGA to control AD9852 directly and then

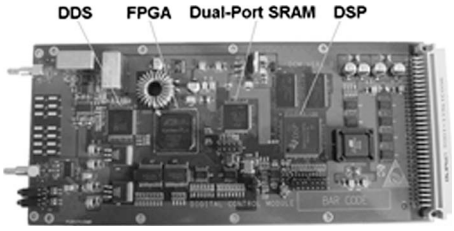

FIG. 3. Photograph of the rf source board.

modifies the relative registers of AD9852 to make it output rf signal with the desired frequency and phase. Finally, it turns on and off the rf switch to generate the hard pulse.

When a soft pulse is needed, the DSP first configures the waveform parameters inside the FPGA (including update period, storage location, and waveform length), then modifies the frequency register of AD9852, then sets the control word to give up the control of AD9852 to the FPGA, and finally sets the control word again to produce a trigger signal and turn on the rf switch. After receiving the trigger signal, the FPGA automatically manipulates AD9852 to generate the desired soft pulse; during this period the DSP can deal with other sequence events.

To generate desired rf signal, the relative registers of AD9852, i.e., FTW (frequency register), POW (phase register) and AMW (amplitude register), should be configured according to Eqs. (1)–(3), as listed below.

The rf signal $s(t)$ can be written as

$$s(t) = A(t)\cos(2\pi ft + \varphi), \quad |A(t)| < 1,$$

then

$$\mathrm{FTW} = (f/\mathrm{sysclk}) \times 2^{48}, \tag{1}$$

where sysclk is the system clock of AD9852 and

$$\begin{cases} \mathrm{POW} = (\varphi/2\pi) \times 2^{14}, & \text{when } A(t) \geq 0 \\ \mathrm{POW} = (\varphi/2\pi + 0.5) \times 2^{14}, & \text{when } A(t) < 0, \end{cases} \tag{2}$$

$$\mathrm{AMW} = |A(t)| \times 2^{12}. \tag{3}$$

The reason for adopting Eqs. (2) and (3) is that registers of AD9852 are unsigned integer and cannot express negative values directly.

IV. EXPERIMENTAL RESULTS

In the present design, there are three sources for the switching time of frequency and phase of the hard pulse: operation time of the DSP, updating time of the DDS, and transmission delay of the analog circuits. The DSP runs a program written in assembly language so as to achieve efficient execution. As mentioned above, the updating time of the DDS is also very short. Meanwhile, the use of rf switch guarantees a small transient delay for turning on and off the hard pulse. Figure 4(a) shows an example of a phase switch with 180° variation, and the hard pulse with turn-on and turn-off states is shown in Fig. 4(b). As illustrated in the diagrams, the phase switching time is less than 400 ns, and the turn-on or turn-off delay does not exceed 100 ns.

Spectral purity is an important performance for a rf source. With a spectrum analyzer of Agilent, Inc. (Santa Clara, California), E4403B, the parameters of the rf source are measured, including phase noise, spurious signal, and noise floor. The spectrum analysis of the output single-tone signal with 21.3 MHz frequency and 1 Vpp amplitude is shown in Fig. 5. The phase noise is 98.6 dBc @ 10 KHz and 138.9 dBc @ 100 KHz, spurious signal is 67.0dBc (±1 MHz), and noise floor is about 140 dBc. The test results show that the rf source has approximately the same phase noise characteristic with a commercial signal generator, such as AFG3021 (Tektronix, Inc., Beaverton, Oregon). According to frequency range and spectral purity, the rf source meets the requirements of low-field (<1 T) MRI and relaxation measurement;[14] in such cases its performance has been validated by experiments.

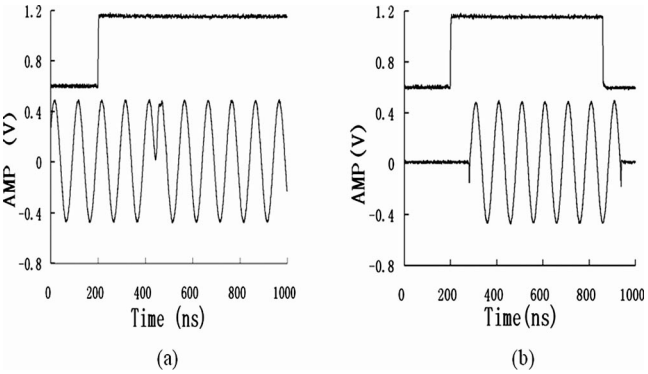

FIG. 4. (a) 180° phase switch of hard pulse; the rising edge of the pulse indicates the time of DSP operation for phase switch. (b) Hard pulse with turn-on and turn-off states; the rising edge of the pulse indicates the time of DSP operation for turn-on, and the falling edge of the pulse indicates the time of DSP operation for turn-off. The frequency of both waveforms is 10 MHz.

Figure 6 shows an experimental result running CPMG sequence in 0.5 T permanent magnetic system in which the tested object is a phantom. Parameters of the experiment are listed as follows: eight echoes with 144 points per echo, spectrometer frequency SF=21.3 MHz, 90° pulse width P90=100 μs, interval between 90° pulse and 180° pulse is 6 ms, signal sampling rate is 50 MHz, and receiving bandwidth is 50 KHz.

The modulation waveform of a soft pulse can be arbi-

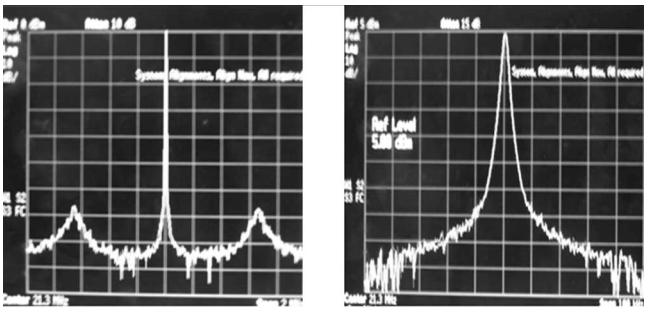

FIG. 5. (a) Image of the spectrum (20.3–22.3 MHz) of the 21.3 MHz single-tone signal with 200 KHz/div horizontal scale, 10 dB/div vertical scale, 0 dBm vertical ref level, and 1 KHz RBW. (b) Image of the spectrum (20.25–22.35 MHz) of the 21.3 MHz single-tone signal with 10 KHz/div horizontal scale, 10 dB/div vertical scale, 5 dBm vertical ref level, and 1 KHz RBW.

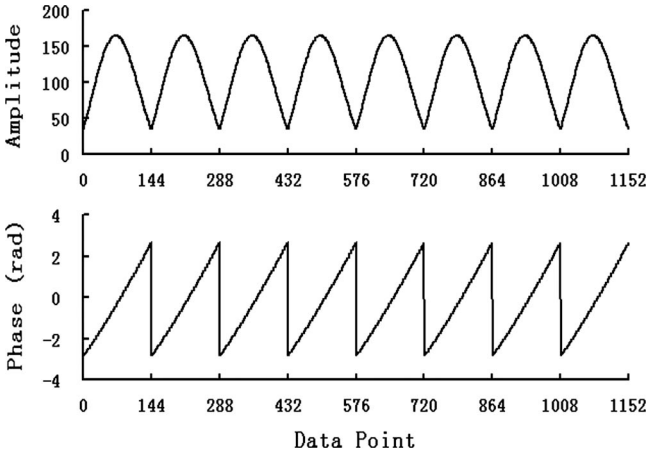

FIG. 6. Received data (modulus and phase) of CPMG echo for a phantom, which is composed of pure water, 0.5% sodium chloride, and 0.11% copper sulfate in 0.5T permanent magnetic system.

trary shape, including sinc, Gaussian, half-Gaussian, and so on. The maximum waveform length is limited to 4096 points in the present design, but it can be expanded with the use of larger dual-port SRAM. Figure 7 shows the soft pulse modulated by waveform 5sinc512, with an update period of 6 μs. Such pulse is usually used in MRI applications.

Figure 8 depicts a T1-weighted image of a round phantom (the same component with the phantom used in the above CPMG experiment) obtained with spin echo pulse sequence in a 0.5 T permanent magnetic system. The soft pulse shown in Fig. 7 is used in this pulse sequence.

V. CONCLUSIONS

In this article, a rf source based on DDS and FPGA is described. The DDS-based architecture achieves short switching time and high resolution in frequency and phase of the rf pulse, and the use of the FPGA optimizes the operation mode of the pulse programmer. The rf source is suitable for being used as transmitter in low-field (<1 T) NMR applications. As a compact and low-cost module, the rf source is of general use for constructing low-field NMR spectrometer.

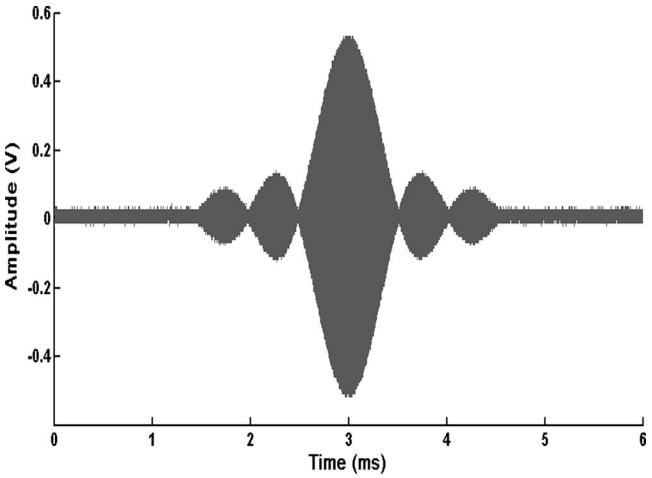

FIG. 7. Soft pulse with modulation waveform 5sinc512; the phase and amplitude are updated every 6 μs with 512 data points. The carrier frequency of the waveform is 21.3 MHz.

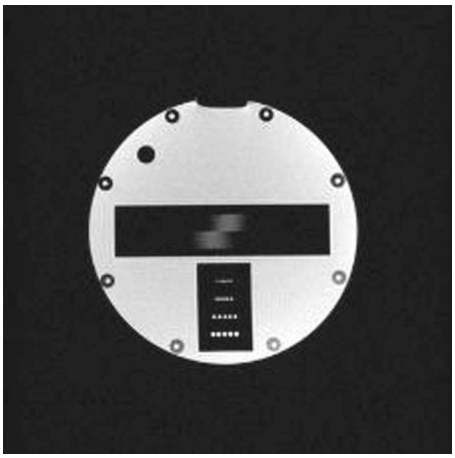

FIG. 8. T1-weighted image of a round phantom (140 mm diameter) obtained with spin echo pulse sequence in a 0.5 T permanent magnetic system. The experiment parameters are as follows: SF=21.3 MHz, P90 =3.072 ms, TR=460 ms, TE=18 ms, number of excitations NEX=2, acquisition matrix size is 256×256, field of view FOV=250×250 mm^2, slice thickness=7 mm, signal sampling rate is 50 MHz, and receiving bandwidth is 50 KHz.

ACKNOWLEDGMENTS

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